WHAT IS CLAIMED IS:

1. A semiconductor die comprising:
   a substrate device level having a substrate pitch; and
   a first above-substrate device level formed above the substrate device level, the first above-substrate device level having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch.

2. The semiconductor die of claim 1 wherein the first above-substrate device level comprises a first plurality of memory cells.

3. The semiconductor die of claim 2 wherein the substrate device level comprises driver circuitry.

4. The semiconductor die of claim 3 wherein the first above-substrate device level comprises:
   a first area, said first area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch; and
   a second area, said second area having a fan-out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch.

5. The semiconductor die of claim 4 wherein the first area comprises a plurality of substantially parallel, substantially coplanar rails.

6. The semiconductor die of claim 5 wherein photolithography processes are optimized to minimize the first above-substrate pitch of the plurality of rails in the first area.

7. The semiconductor die of claim 6 wherein the plurality of rails is patterned using off-axis illumination.

8. The semiconductor die of claim 7 wherein the plurality of rails is patterned using a dipole illumination aperture.

9. The semiconductor die of claim 5 wherein the die includes dummy structures.

10. The semiconductor die of claim 5 further comprising a second above-substrate device level formed over the first above-substrate device level, the second above-substrate device level having a second above-substrate pitch, wherein the second above-substrate pitch is smaller than the substrate pitch.

11. The semiconductor die of claim 5 wherein the rails comprise a first plurality of memory lines electrically connected to a first plurality of vertical interconnects at a first end and a second plurality of memory lines electrically connected to a second plurality of vertical interconnects at a second end opposite the first end, the first and second pluralities interleaved.

12. The semiconductor die of claim 2 wherein the plurality of memory cells form part of a monolithic three dimensional memory array.

13. The semiconductor die of claim 12 wherein the memory array comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line.

14. The semiconductor die of claim 12 wherein the memory array comprises word lines segments and a word line driver circuit in the substrate.

15. The semiconductor die of claim 2 wherein the memory cells are passive element memory cells.

16. The semiconductor die of claim 16 wherein the memory cells are antifuse-diode cells.

17. The semiconductor die of claim 2 wherein the memory cells are thin film transistors having a charge-storage dielectric.

18. The semiconductor die of claim 17 wherein the memory cells are arranged in series-connected NAND strings.

19. A semiconductor die comprising:

a substrate device level having a substrate pitch; and

a first memory level above a substrate having a first memory pitch, wherein the first memory pitch is smaller than the substrate pitch.

20. The semiconductor die of claim 19 wherein the substrate device level comprises driver circuitry.

21. The semiconductor die of claim 19 further comprising a second memory level above the first memory level, the second memory level having a second memory pitch, wherein the second memory pitch is smaller than the substrate pitch.

22. The semiconductor die of claim 19 wherein the first memory level comprises a plurality of substantially parallel, substantially coplanar rails.

23. The semiconductor die of claim 22 wherein the rails comprise a first plurality of memory lines electrically connected to a first plurality of vertical interconnects at a first end and a second plurality of memory lines electrically connected to a second plurality of vertical interconnects at a second end opposite the first end, the first and second pluralities interleaved.

24. A monolithic three dimensional memory array comprising:

a substrate device level comprising devices formed in a substrate having a first pitch; and

a first memory level formed over the substrate device having a second pitch, wherein the second pitch is smaller than the first pitch.

25. The monolithic three dimensional memory array of claim 24 further comprising a second memory level formed over the first memory level, the second memory level having a third pitch, wherein the third pitch is smaller than the first pitch.

26. The monolithic three dimensional memory array of claim 25 wherein the first memory level comprises a plurality of substantially parallel, substantially coplanar semiconductor rails.

27. The monolithic three dimensional memory array of claim 25 further comprising at least a third memory level formed over the second memory level, the third memory level having a fourth pitch, wherein the fourth pitch is smaller than the first pitch.

28. The monolithic three dimensional memory array of claim 24 further comprising memory cells, wherein the memory cells are passive element memory cells.

29. The monolithic three dimensional memory array of claim 28 wherein the memory cells are antifuse-diode cells.

30. The monolithic three dimensional memory array of claim 24 further comprising memory cells, wherein the memory cells are thin film transistors having a charge-storage dielectric.

31. The monolithic three dimensional memory array of claim 30 wherein the memory cells are arranged in series-connected NAND strings.

32. The monolithic three dimensional memory array of claim 24 further comprising segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line.

33. The monolithic three dimensional memory array of claim 24 further comprising word lines segments and a word line driver circuit in the substrate.

34. A semiconductor die comprising:

a first device level formed in a substrate, the first device level having a first pitch; and

a first plurality of substantially parallel, substantially coplanar rails formed above the substrate, the first plurality of rails having a second pitch, wherein the first pitch is larger than the second pitch.

35. The semiconductor die of claim 34 wherein the first device level comprises CMOS circuitry.

36. The semiconductor die of claim 35 wherein portions of the rails form diode portions.

37. The semiconductor die of claim 36 wherein portions of the rails form gate electrodes.

38. The semiconductor die of claim 36 wherein portions of the rails form transistor bodies.

39. The semiconductor die of claim 34 wherein the rails comprise a first plurality of memory lines electrically connected to a first plurality of vertical interconnects at a first end and a second plurality of memory lines electrically connected to a second plurality of vertical interconnects at a second end opposite the first end, the first and second pluralities of memory lines interleaved.

40. A semiconductor device level comprising:

a first area comprising a plurality of substantially parallel, substantially coplanar rails, the first plurality of rails having a first pitch; and

a second area having a second pitch, wherein the second pitch is larger than the first pitch,

wherein photolithographic techniques optimized for forming rails are used to pattern the semiconductor device level.

41. The semiconductor device level of claim 40 wherein the device level is formed above a substrate.

42. The semiconductor device level of claim 41 wherein a substrate device level is formed in the substrate.

43. The semiconductor device level of claim 41 wherein the substrate device level comprises CMOS circuits.

44. The semiconductor device level of claim 43 wherein the CMOS circuits have a substrate pitch, the substrate pitch greater than the first pitch.

45. The semiconductor device level of claim 42 wherein the device level comprises memory cells.

46. A semiconductor die comprising:

a substrate device level having a substrate critical dimension; and

a first above-substrate device level formed above the substrate device level, the first above-substrate device level having a first above-substrate critical dimension, wherein the first above-substrate critical dimension is smaller than the substrate critical dimension.

47. The semiconductor die of claim 46 wherein the die includes dummy structures.

48. The semiconductor die of claim 46 wherein the first above-substrate device level comprises a first plurality of memory cells.

49. The semiconductor die of claim 48 wherein the memory cells are passive element memory cells.

50. The semiconductor die of claim 49 wherein the memory cells are antifuse-diode cells.

51. The semiconductor die of claim 48 wherein the memory cells are thin film transistors having a charge-storage dielectric.

52. The semiconductor die of claim 51 wherein the memory cells are arranged in series-connected NAND strings.

53. The semiconductor die of claim 48 wherein the substrate device level comprises driver circuitry.

54. The semiconductor die of claim 53 wherein the first above-substrate device level comprises:

a first area, said first area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate critical dimension; and

a second area, said second area having a fan-out critical dimension, wherein said fan-out critical dimension is larger than the first above-substrate critical dimension.

55. The semiconductor die of claim 54 wherein the first area comprises a plurality of substantially parallel, substantially coplanar rails.

56. The semiconductor die of claim 55 wherein the rails comprise a first plurality of memory lines electrically connected to a first plurality of vertical interconnects at a first end and a second plurality of memory lines electrically connected to a second plurality of vertical interconnects at a second end opposite the first end, the first and second pluralities interleaved.

57. The semiconductor die of claim 55 wherein photolithography processes are optimized to minimize the first above-substrate critical dimension of the plurality of rails in the first area.

58. The semiconductor die of claim 55 further comprising a second above-substrate device level formed over the first above-substrate device level, the second above-substrate device level having a second above-substrate critical dimension, wherein the second above-substrate critical dimension is smaller than the substrate critical dimension.

59. The semiconductor die of claim 48 wherein the plurality of memory cells form part of a monolithic three dimensional memory array.